Silicon Spin Qubits in Quantum Dots Physics

Pauli Spin Blockade Singlet-Triplet Readout, Exchange Coupling J-Gate Control, and Cryo-CMOS

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EXECUTIVE ABSTRACT: Superconducting transmon qubits face a fundamental interconnect bottleneck due to millimeter-scale footprint constraints and millikelvin dilution refrigeration limits. Silicon spin qubits confined in electrostatically defined quantum dots offer nanometer-scale footprint (50 nm pitch) and 1.2K operation. This dossier audits isotopic 28Si decoherence, exchange coupling, and Cryo-CMOS integration.

Physical Parameter	Superconducting Transmon	Silicon Spin Qubit (28Si)
Physical Qubit Footprint	1 mm × 1 mm (Bulk Macro)	50 nm × 50 nm (Quantum Dot)
Operating Temperature	15 millikelvin (mK)	1.2 Kelvin (High-Temp Regime)
Dephasing Time (T2*)	80 - 150 microseconds	120 microseconds (Purified 28Si)
Two-Qubit Gate Fidelity	99.8% (Cross-Resonance)	99.5% (Exchange J-Gate)
Control Interconnect Scaling	2 Coaxial Cables / Qubit	Cryo-CMOS Multiplexed Matrix

1. Isotopically Purified 28Si and Hyperfine Decoherence Mitigation

Natural silicon contains 4.7% of the 29Si isotope, whose nuclear spin creates fluctuating Overhauser magnetic fields that decohere electron spins within 10 nanoseconds. Purifying silicon to less than 50 ppm 29Si suppresses magnetic noise, expanding electron dephasing times (T_2^*) past 120 microseconds.

2. Pauli Spin Blockade (PSB) and Single-Shot Singlet-Triplet Readout

Readout utilizes Pauli Spin Blockade in a double quantum dot. When two electrons occupy adjacent dots, interdot tunneling is strictly forbidden if their spins form a parallel triplet state, but permitted if they form an antiparallel singlet state. An adjacent Single-Electron Transistor (SET) senses charge displacement with 99.2% fidelity.

3. Exchange Coupling J(ε) Electrostatic Gate Dynamics

Two-qubit logic gates rely on exchange interaction $J(\epsilon) \propto \exp(-\Delta V)$, controlled by nanosecond voltage pulses on electrostatic barrier gates between dots. Tuning gate voltage modulates the wave-function overlap, enabling controlled-phase (CZ) gate execution within 12 nanoseconds.

4. 1.2 Kelvin Operation and Co-Integrated Cryo-CMOS Multiplexers

Unlike transmons confined to 15 mK where cooling power is limited to microwatts, silicon spin qubits operate at 1.2 Kelvin, where cryocoolers deliver watts of thermal lift. Standard 300mm FD-SOI foundries can co-fabricate cryo-CMOS control multiplexers alongside qubit arrays, routing millions of qubits over fewer than 100 coaxial leads.

STRATEGIC ARCHITECTURAL CONCLUSIONS:

- Silicon spin qubits boast a physical footprint 10,000x smaller than superconducting transmons, enabling million-qubit monolithic integration.
- Isotopic purification to 28Si eliminates Overhauser nuclear spin decoherence, extending electron spin coherence into the millisecond regime.
- Operation at 1.2 Kelvin enables direct on-die co-integration with silicon Cryo-CMOS control electronics, resolving the quantum wiring bottleneck.