Cryogenic Ferroelectric FETs (Cryo-FeFET) for Quantum Qubit Control

4-Kelvin Carrier Freeze-Out Suppression, HZO Polarization Stability, and Nanowatt Readout Power Budgets

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EXECUTIVE ABSTRACT: *Scaling superconducting and spin-qubit quantum processors beyond 1,000 qubits is severely throttled by the 'wiring bottleneck'—routing individual coaxial RF cables from room-temperature controllers down to the 15-millikelvin dilution refrigerator stage. Monolithic Cryo-CMOS control electronics placed at the 4-Kelvin stage solve this bottleneck. Cryogenic Ferroelectric FETs (Cryo-FeFET) utilizing doped HfO2 dielectrics overcome carrier freeze-out, providing non-volatile local qubit state memory and ultra-low-power microwave multiplexing.*

Physical Parameter	Cryo-FeFET (4.2 Kelvin)	Standard Cryo-MOSFET (4.2K)	Room-Temp CMOS Control
Carrier Freeze-Out Effect	Suppressed via Electric Field	Severe Ionization Dropoff	None (300 Kelvin)
Subthreshold Swing (SS)	14.2 mV / decade (Steep slope)	32.0 mV / decade	75.0 mV / decade
Non-Volatile Memory Retention	>10 Years at 4.2 K	Volatile (Requires constant refresh)	Standard Non-Volatile Flash
Thermal Dissipation Budget	<120 uW per Readout Channel	1.2 - 2.5 mW per Channel	External (Cables generate heat)

1. The Quantum Cryostat Wiring Bottleneck

State-of-the-art dilution refrigerators provide only 10 to 20 microWatts of cooling lift at the 15 mK mixing chamber and ~1.5 Watts at the 4.2 K intermediate stage. Standard quantum architectures routing hundreds of coaxial lines suffer parasitic passive thermal conduction and active RF attenuation, physically capping processor scaling. Placing autonomous control and readout logic directly at the 4K stage is the only viable path to 100,000-qubit systems.

2. Cryogenic Carrier Freeze-Out Physics

At 4 Kelvin, standard silicon CMOS encounters carrier freeze-out: thermal energy k_B * T drops below the dopant ionization energy (e.g., 45 meV for Boron in Si), trapping conduction electrons in parent impurity atoms and causing dramatic threshold voltage shifts, kink effects, and carrier mobility collapse. FeFETs overcome freeze-out by leveraging the intense remanent polarization field of ferroelectric Hf_{0.5}Zr_{0.5}O_2 (HZO) gate stacks to ionize carriers electrostatically.

3. HZO Ferroelectric Polarization Dynamics at 4K

Orthorhombic-phase HZO films exhibit robust remanent polarization P_r ~ 24 uC/cm^2 that remains exceptionally stable down to 100 millikelvin. Unlike floating-gate Flash memory, which suffers carrier freeze-out and high programming voltages at cryogenic temperatures, FeFET polarization switching is purely displacive (sub-picometer shift of oxygen atoms within the unit cell), requiring low write voltages (<2.5V) and zero thermal activation energy.

4. Local Qubit Memory & Multiplexed Microwave Drive

Cryo-FeFET arrays store calibration parameters, arbitrary waveform generator (AWG) microcode, and error-correction lookup tables locally at the 4K stage. This enables dynamic frequency-division multiplexing where a single coaxial cable controls 64 to 128 individual qubits, reducing the total wiring harness diameter by 90% while adhering strictly to the 1.5W cryostat thermal budget.

Key Strategic Architecture Takeaways

- Cryo-FeFETs placed at the 4-Kelvin stage resolve the cryogenic wiring bottleneck for large-scale quantum computers.
- Electrostatic polarization fields from ferroelectric HZO suppress cryogenic silicon dopant carrier freeze-out.
- Subthreshold swing sharpens to 14.2 mV/dec, enabling low-voltage, sub-120 uW analog-to-digital converter channels.
- Displacive non-volatile polarization switching enables in-situ AWG waveform storage with sub-2.5V operating budgets.