TECHNICAL DOSSIER // SEMICONDUCTOR PHYSICS & NANOELECTRONICS

2D Transition Metal Dichalcogenide Sub-1nm Gate Transport

Monolayer Channel Electrostatics, Van der Waals Contacts, and High-k Dielectric Integration

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EXECUTIVE SUMMARY & MICROARCHITECTURAL SCOPE

As silicon Gate-All-Around (GAA) nanosheets approach their fundamental physical scaling barrier at sub-10nm channel lengths, severe quantum source-to-drain direct tunneling and surface scattering degrade device subthreshold swing. Atomic monolayer transition metal dichalcogenides (TMDs)—specifically MoS2 and WSe2—provide sub-nanometer body thickness (0.65 nm) without dangling surface bonds, enabling pristine gate electrostatics with subthreshold swings below 65 mV/dec and effective oxide thickness (EOT) under 0.5 nm.

Parameter	Bulk Silicon (3nm)	Si GAA Nanosheet	Monolayer MoS2	Monolayer WSe2
Channel Thickness	5.0 nm	3.0 nm	0.65 nm	0.70 nm
Direct Bandgap	1.12 eV (Indirect)	1.12 eV	1.80 eV (Direct)	1.65 eV (Direct)
Subthreshold Swing	78 mV/dec	68 mV/dec	64 mV/dec	63 mV/dec
Contact Resistance	40 Ohm-um	65 Ohm-um	123 Ohm-um (Bi)	145 Ohm-um (Pt)
Drive Current (I_on)	1.8 mA/um	1.5 mA/um	1.25 mA/um	1.10 mA/um

1. Electrostatic Scaling and Quantum Tunneling Suppression

At channel lengths below 12 nm, three-dimensional bulk silicon transistors suffer from uncontrollable source-to-drain direct band-to-band tunneling and drain-induced barrier lowering (DIBL). In contrast, two-dimensional monolayer TMDs possess an atomically thin body thickness t_ch = 0.65 nm, yielding a natural scaling length lambda = sqrt((epsilon_ch / epsilon_ox) * t_ch * t_ox) that suppresses short-channel effects even when gate lengths scale down to 1 nm.

2. Van der Waals Semimetal Contacts & Fermi Level Pinning

The primary engineering obstacle in TMD FETs has been high contact resistance (Rc > 10,000 Ohm-um) caused by Fermi level pinning near the conduction band edge due to metal-induced gap states (MIGS). Modern fabrication utilizes semimetallic contacts—specifically bismuth (Bi) and antimony (Sb)—that suppress quantum mechanical wave-function overlap at the van der Waals interface, achieving near-zero Schottky barrier heights and contact resistances down to 123 Ohm-um.

3. Top-Gate High-k Dielectric Integration

Integrating sub-0.5 nm EOT dielectrics directly onto pristine MoS2 requires solving the absence of surface dangling bonds, which traditionally impedes atomic layer deposition (ALD). Modern fab recipes deposit sub-nanometer aluminum seed layers oxidized into Al2O3 or crystalline HfO2 via low-temperature plasma-enhanced ALD, preventing interfacial trap density (Dit) spikes and preserving field-effect electron mobility above 80 cm^2/V-s.

4. Complementary 2D Logic: n-type MoS2 and p-type WSe2

Achieving complementary logic (CFET) necessitates pairing n-FET MoS2 channels with high-performance p-FET channels. Monolayer Tungsten Diselenide (WSe2) exhibits high hole mobility (~120 cm^2/V-s) when contacted with high work-function noble metals like platinum or oxidized ruthenium, enabling vertically stacked 3D monolithic complementary logic gates with 40% area reduction over 2nm CFET.

STRATEGIC ENGINEERING TAKEAWAYS & DEPLOYMENT CHECKLIST

- **Sub-1nm Channel Integrity:** Monolayer body thickness eliminates short-channel leakage and source-to-drain quantum tunneling.
- **Semimetal Bi/Sb Contacts:** Reduces contact resistance below 150 Ohm-um by eliminating Fermi level pinning.
- **ALD High-k Integration:** Engineered seed layers permit sub-0.5 nm EOT HfO2 gate oxides without degrading 2D mobility.
- **Complementary CFET Stacking:** MoS2 n-FETs and WSe2 p-FETs establish the foundation for post-silicon sub-1nm CMOS standard cells.