TECHNICAL DOSSIER // HARDWARE & DEVICES

Photonic Tensor Processors: Electro-Optic MZIs vs. Digital Systolic Arrays

Silicon Photonics Unitary Decompositions, Optical Propagation Physics, and Scaling Limits

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EXECUTIVE SUMMARY & MICROARCHITECTURAL SCOPE

This engineering dossier investigates co-packaged electro-optic Mach-Zehnder Interferometer (MZI) meshes for artificial intelligence matrix-vector multiplications. By mapping weight matrices onto unitary Clements triangular optical meshes via Singular Value Decomposition, photonic tensor processors perform analog linear algebra at the speed of light with sub-picosecond propagation delays, circumventing RC wire capacitance bottlenecks while confronting electro-optic DAC/ADC domain conversion and phase drift challenges.

Architecture Metric	Digital Systolic Array (4nm)	Photonic MZI Mesh (Silicon)	Hybrid Opto-Electronic (Co-Packaged)
Energy Efficiency (MAC)	1.5 to 3.5 pJ / MAC	< 0.05 pJ / MAC (Optical)	0.35 to 0.65 pJ / MAC (System)
Transit Latency (64x64)	15 to 40 ns (Pipelined)	< 0.15 ns (Speed of Light)	1.2 to 2.5 ns (ADC+Laser+Det)
Thermal Sensitivity	Low (< 0.5% drift / 10°C)	High (Thermo-optic drift)	Medium (Pockels phase feedback)
Weight Precision	INT8 / FP8 / FP16 exact	6 to 8-bit analog ENOB	8-bit hybrid optical MAC

1. The Interconnect Capacitance Wall in Digital Linear Algebra

Modern deep learning silicon architectures rely on large 2D systolic arrays of multiply-accumulate (MAC) units. While floating-point ALUs continue to scale with advanced lithography, digital interconnect wires incur static RC time constants and capacitive charging dissipation (E = 0.5 * C * V^2 * f). In high-density AI accelerators, over 70% of total silicon package power is lost directly to metal line parasitic charging and SRAM register file transfers rather than arithmetic logic.

2. Electro-Optic Mach-Zehnder Interferometer Meshes

Photonic tensor processors replace resistive copper wires with optical silicon waveguides. An MZI consists of a 50:50 input beam splitter, two parallel waveguide arms, internal phase modulators, and an output combiner. By applying an electric field via thermo-optic heaters or carrier-depletion electro-optic phase shifters, the optical phase difference theta and phi modulates optical interference, realizing an exact 2x2 complex unitary rotation.

3. Unitary Matrix Decomposition & The Clements Mesh Topology

Any arbitrary N x N unitary transformation U can be physically decomposed into a triangular (Reck) or rectangular (Clements) mesh of N(N-1)/2 tunable MZIs. Using Singular Value Decomposition (M = U * Sigma * V*), an arbitrary weight matrix M is synthesized optically using two unitary MZI meshes separated by an optical attenuation array Sigma. The matrix multiplication occurs passively as coherent laser photons propagate through the mesh at ~10^8 m/s in silicon.

4. The Electro-Optic Domain Conversion Bottleneck

Despite sub-picosecond optical matrix calculation, photonic processors face severe electro-optic conversion overheads. Digital inputs must be converted into analog voltages via high-speed DACs, modulated onto optical carriers, detected by high-responsivity Ge-on-Si photodiodes, and digitized by transimpedance amplifiers and ADCs. System efficiency hinges on co-packaged optics (CPO) and high-density microbumps to eliminate parasitic PCB trace capacitance.

STRATEGIC ENGINEERING TAKEAWAYS & DEPLOYMENT CHECKLIST

• **Passive Optical MAC Efficiency:** Optical matrix transit consumes negligible energy; system power is dominated entirely by DAC, laser diode, and ADC conversion circuits.
• **Phase Calibration Stability:** Active thermal feedback loops or non-volatile phase-change materials (e.g., GST/GSST) are mandatory to mitigate silicon refractive index thermal drift.
• **Target AI Deployment:** Photonic processors excel in high-throughput, latency-critical inference pipelines (e.g., LLM prefill and batch-1 autoregressive decoding).