

# PCIe Gen 6 PAM4 Signaling, Flit Architecture & FEC Overhead

High-Speed Interconnect Physics: 66% Eye Collapse, Retransmissions, and Latency Jitter

Published by *Lesty Tech High-Speed Interconnect Lab* | Date: October 20, 2026 | Reference: LESTY-ENG-2026-B6

## 1. The High-Speed Electrical Boundary of NRZ Signaling

From PCIe 1.0 through PCIe 5.0, high-speed peripheral interconnects relied on Non-Return-to-Zero (NRZ) binary signaling, transmitting one bit per clock cycle using two electrical voltage levels. At PCIe Gen 5's 32 GT/s line rate, the Nyquist frequency reaches 16 GHz. In standard server motherboards with FR4 or low-loss Megtron dielectric substrates, insertion loss at 16 GHz exceeds 36 dB across a 14-inch PCB trace. Doubling NRZ to 64 GT/s would have pushed the Nyquist frequency to 32 GHz, causing extreme dielectric absorption where signals decay into unrecognizable electrical noise within 3 inches.

## 2. PAM4 Modulation Physics and the 66% Eye Height Collapse

*Physical Layer Reality: PCIe Gen 6 maintains the 16 GHz Nyquist frequency while doubling raw throughput to 64 GT/s by adopting 4-level Pulse Amplitude Modulation (PAM4). By transmitting two bits per baud across four discrete voltage levels (00, 01, 10, 11), PAM4 doubles bandwidth at identical cycle times. However, dividing the 1-volt signal swing into four distinct bands slashes the eye height voltage margin by 66% (from 1000mV to ~333mV), causing the raw Bit Error Rate (BER) to skyrocket from 10<sup>-12</sup> to 10<sup>-4</sup>.*

## 3. Mandatory Flit Mode, Forward Error Correction, and Latency Jitter

Because PAM4 links generate constant background bit errors, PCIe 6 mandates 256-byte Flow Control Unit (Flit) packetization and lightweight Forward Error Correction (FEC). The Reed-Solomon RS(242, 230) FEC engine corrects up to 6 symbol errors per flit, reducing the post-FEC error rate to safe levels. However, decoding FEC and processing Cyclic Redundancy Checks (CRC) adds ~10ns of mandatory physical serialization delay, and high-noise environments trigger replay buffer retransmissions that cause microsecond-level latency spikes.

## ARCHITECTURAL BENCHMARK & PARAMETER TELEMETRY

| Interconnect Standard    | PCIe Gen 4                            | PCIe Gen 5                            | PCIe Gen 6 (PAM4)                                    |
|--------------------------|---------------------------------------|---------------------------------------|------------------------------------------------------|
| Modulation Scheme        | NRZ (2 Voltage Levels)                | NRZ (2 Voltage Levels)                | PAM4 (4 Voltage Levels)                              |
| Raw Data Rate            | 16 GT/s per lane                      | 32 GT/s per lane                      | 64 GT/s per lane                                     |
| Nyquist Frequency        | 8.0 GHz                               | 16.0 GHz                              | 16.0 GHz (Maintained)                                |
| Eye Opening Margin       | 100% Full Eye                         | 100% Full Eye                         | 33% Eye Height (-66% margin)                         |
| Raw Bit Error Rate (BER) | < 10 <sup>-12</sup> (Near error-free) | < 10 <sup>-12</sup> (Near error-free) | 10 <sup>-4</sup> to 10 <sup>-5</sup> (Severe errors) |

|                    |                      |                      |                              |
|--------------------|----------------------|----------------------|------------------------------|
| FEC / CRC Overhead | Zero (No FEC needed) | Zero (No FEC needed) | Mandatory 256B Flit + RS-FEC |
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