

NVMe NAND Flash Architecture and SLC Caching Whitepaper

Analyzing Voltage Distribution States, Dynamic Cache Depletion, and Folding Latencies

Author: Lesty Tech Storage Systems Team | Date: October 2026 | Verified Technical Documentation

1. The Multi-Bit Cell Paradox: TLC vs. QLC

Modern high-capacity NVMe SSDs utilize 3D TLC (Triple-Level Cell, 3 bits/cell) or QLC (Quad-Level Cell, 4 bits/cell) flash memory. Storing 4 bits in a single microscopic floating-gate or charge-trap capacitor requires distinguishing between 16 precise voltage threshold states.

Programming 16 distinct voltage states requires iterative program-and-verify pulses (ISPP). Consequently, native QLC sequential write throughput is inherently slow: between 80 MB/s and 160 MB/s per die.

NOTE: Consumer SSDs mask this sluggish native speed by dynamically allocating up to one-third of available free space as a high-speed pseudo-SLC cache.

2. The Two-Stage SLC Folding Collapse

During sustained write bursts (such as transferring a 300GB video archive or restoring database snapshots), the dynamic pseudo-SLC cache is completely saturated.

When the cache is exhausted, the SSD controller enters the 'folding state.' The controller must simultaneously service incoming host write requests while reading existing 1-bit SLC blocks, calculating parity, and compressing them into dense 4-bit QLC blocks.

CRITICAL: Channel contention and flash programming latency cause sustained write speeds to collapse by up to 95%, dropping 7,000 MB/s Gen 4 drives down to 180 MB/s.

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Performance Metric	Burst Mode (Pseudo-SLC)	Sustained Mode (Exhausted / Folding)
Sequential Write Speed	6,800 - 7,200 MB/s	160 - 240 MB/s (-96%)
Voltage Threshold Levels	2 States (1 bit)	16 States (4 bits)
Write Amplification Factor	1.05 - 1.20	2.80 - 4.10 (Severe wear)
Controller Channel Latency	< 35 microseconds	> 850 microseconds

Sustained Cache Recovery	Immediate on idle	Requires 10-15 min idle GC
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