

Glass Substrates & Next-Gen Advanced Semiconductor Packaging

Engineering Dossier: Overcoming Organic ABF Core Warpage, Through-Glass Vias (TGV), and Reticle Scaling Limits

Published by Lesty Tech Hardware Architecture Group • Date: October 21, 2026 • Lesty.tech Architectural Engineering Dossier

1. The Mechanical Scaling Cliff of Organic ABF Substrates

For three decades, high-performance computing chip packaging has relied on organic core substrates built with bismaleimide-triazine (BT) resin and Ajinomoto Build-up Film (ABF). However, as multi-chiplet AI accelerators scale package footprints past 100mm x 100mm (accommodating >4x reticle sizes), organic cores suffer severe physical warpage. The mismatched Coefficient of Thermal Expansion (CTE) between silicon (2.6 ppm/K) and organic cores (15-18 ppm/K) induces thermal stress that fractures microbumps and delaminates die interfaces during reflow.

2. Physical and Material Advantages of Fused Silica Glass

Glass substrates (borosilicate and fused silica) offer an adjustable CTE (3.0 to 9.0 ppm/K) closely matching silicon, eliminating thermal warpage during packaging assembly. Glass delivers extreme mechanical rigidity with an elastic modulus exceeding 70-80 GPa, and ultra-high surface flatness (roughness Ra < 0.1 nm). These physical properties enable direct sub-micron lithographic patterning with line/space (L/S) dimensions dropping from 10/10 um down to 1/1 um.

3. Through-Glass Via (TGV) Laser Drilling and Metallization

Unlike organic substrates that rely on mechanical or UV laser ablation, glass vias are formed using advanced laser-induced deep etching (LIDE). Picosecond pulsed lasers induce localized structural phase transitions in the glass, followed by selective chemical etching that creates pristine, taper-free Through-Glass Vias (TGVs) with pitch scaling below 10-20 microns and aspect ratios exceeding 10:1 to 20:1.

4. Thermal Conductivity Paradox and Co-Packaging Integration

While glass exhibits lower bulk thermal conductivity (~1.0 to 1.4 W/m.K) compared to silicon (140 W/m.K), glass serves exclusively as a structural and electrical redistribution substrate; heat is extracted vertically from the top of the silicon chiplets via direct cold plates. Furthermore, glass's optical transparency opens the frontier for co-packaged optical waveguides embedded directly within the glass core substrate.

Key Engineering Metrics & Reference Specifications

Packaging Parameter	Organic ABF Core	Silicon Interposer (CoWoS-S)	Glass Substrate Core
---------------------	------------------	------------------------------	----------------------

Max Substrate Area	100 x 100 mm (Warp Limit)	~3.3x Reticle (80 x 80 mm)	Up to 510 x 515 mm Panel
Coefficient of Thermal Expansion	15 - 18 ppm/K	2.6 ppm/K	3.0 - 8.5 ppm/K (Tunable)
Surface Flatness (Ra)	~20 - 50 nm	< 0.5 nm	< 0.1 nm (Atomic Flatness)
Via Pitch Capability	50 - 100 um (PTH)	10 - 25 um (TSV)	10 - 30 um (TGV)
Dielectric Loss Tan (10 GHz)	0.015 - 0.020	High (Lossy Si)	0.003 - 0.005 (Ultra-Low)

Engineering Notice: This whitepaper is an official technical companion resource released in conjunction with Lesty.tech research publications. All structural schematics, formulas, and empirical microarchitectural data are strictly verified against IEEE, JEDEC, USENIX, and ACM research standards.