

GAAFET Nanosheet Architecture & Bottom Dielectric Isolation

Engineering Report on Sub-Channel Punch-Through Leakage and BDI in Sub-2nm Silicon

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1. Executive Summary & Sub-2nm Physics Bottleneck

As semiconductor fabrication transitions from FinFET 3D fins to vertically stacked Gate-All-Around Nanosheet FETs (GAAFET / Intel RibbonFET / TSMC N2 / Samsung SF3), electrostatic control over channel inversions significantly improves. However, moving to horizontally stacked channels introduces an unmitigated parasitic phenomenon: bottom sub-channel punch-through leakage into the underlying bulk silicon substrate. Without an insulating boundary beneath the bottommost nanosheet, up to 28% of total transistor off-state leakage (I_{off}) bypasses the gate, causing catastrophic static power dissipation in sub-0.7V threshold regimes.

2. The Bottom Dielectric Isolation (BDI) Engineering Mechanism

Critical Architectural Reality: Gate-All-Around architecture physically wraps four sides of the nanosheet channel wires, but conventional epitaxy leaves the bottom source/drain region directly coupled to the bulk substrate. Bottom Dielectric Isolation (BDI) introduces an atomic layer SiO2/SiN dielectric floor directly underneath the bottom sheet via selective lateral isotropic etching of a sacrificial SiGe layer, completely severing parasitic sub-channel capacitive coupling.

3. Thermal Dissipation Trade-offs and Stress Engineering

While BDI reduces bottom channel parasitic capacitance (C_{par}) by 35% and improves $I_{\text{on}}/I_{\text{off}}$ ratios by an order of magnitude, SiO2 possesses a thermal conductivity of only 1.4 W/m·K (compared to 148 W/m·K for monocrystalline bulk silicon). Inserting this dielectric barrier creates a localized thermal insulator that increases transistor channel hot-spot peak temperatures by 12–18°C under continuous vector workloads, necessitating optimized thermal vias and back-side metal heat sinks.

ARCHITECTURAL BENCHMARK & PARAMETER TELEMETRY

Process Parameter	FinFET (TSMC N3E)	GAAFET without BDI	GAAFET with BDI (N2)
Channel Architecture	Vertical 3D Fin (34nm H)	3-Tier Stacked Nanosheet	3-Tier Stacked Nanosheet + BDI
Sub-Channel Leakage (I_{off})	Baseline Ref (~10 nA/um)	+45% Punch-Through Risk	-78% (Severed bulk path)
Parasitic Capacitance (C_{par})	0.85 fF/um	1.18 fF/um (High bottom loss)	0.72 fF/um (-39% reduction)
Channel Peak Temperature	68°C under 1.1V load	74°C (Moderate bulk dissipation)	89°C (+15°C localized phonon trap)
Minimum Gate Pitch (CPP)	48 nm	45 nm	42 nm

