

Complementary FET (CFET) 3D Transistor Architecture

Monolithic Nanosheet Stacking, 1.5-Track Cell Scaling, and Mol Backside Routing Physics

EXECUTIVE ABSTRACT & SUMMARY FINDINGS: As gate-all-around (GAAFET) nanosheets reach scaling walls at the A14 (1.4nm) node due to contacted poly pitch (CPP) limits and horizontal n-to-p transistor spacing, Complementary FET (CFET) emerges as the defining architecture for post-2026 silicon. By vertically folding pFET nanosheets directly above nFET channels, CFET achieves a 50% standard cell footprint reduction. This dossier audits monolithic vs. sequential fabrication, high-aspect-ratio etching constraints, parasitic thermal dissipation, and dual-side power delivery networks.

Architecture	Cell Height	n-to-p Spacing	Transistor Density
FinFET (3nm)	5.0T (150nm)	15nm - 22nm	1.0x (Baseline)
GAAFET (2nm)	3.0T (90nm)	10nm - 14nm	1.65x - 1.85x
Sequential CFET (1nm)	2.0T (60nm)	Vertical Wafer Bond	2.40x - 2.70x
Monolithic CFET (A10)	1.5T (45nm)	0nm (Self-Aligned)	3.10x - 3.45x

1. The Horizontal GAAFET Bottleneck and the 1.5-Track Scaling Limit

Silicon scaling has historically advanced by reducing gate pitch and standard cell track height. However, GAA nanosheets cannot scale below 3-track height in standard planar layouts because the n-type and p-type nanosheets sit adjacent to one another on the wafer surface. The minimum spacing between nFET and pFET regions (n-to-p separation) is governed by isolation oxide deposition and dummy gate cut boundaries, which stall at approximately 12nm.

Complementary Field-Effect Transistors (CFET) demolish this geometric ceiling by rotating the n-to-p boundary from the horizontal plane to the vertical Z-axis. By placing the pFET nanosheet stack directly on top of the nFET stack (or vice versa), the horizontal separation collapses to zero. Standard cells that historically required 6 metal tracks collapse into 3 or 2 tracks, cutting logic cell area by 45% to 52% without forcing aggressive gate pitch scaling.

2. Monolithic vs. Sequential CFET: Fabrication Complexities & Aspect Ratios

Foundries are pursuing two distinct CFET paradigms: Monolithic and Sequential (3D CoolCube). Monolithic CFET epitaxially grows alternating superlattices of Si and SiGe (e.g., Si/SiGe/Si/SiGe/Si/SiGe) in a single run, then selectively etches SiGe to release both upper and lower nanosheet channels. This requires ultra-high-aspect-ratio reactive ion etching (HAR-RIE) through trenches exceeding 120nm in depth with sub-1nm sidewall verticality.

Sequential CFET instead processes the bottom transistor on a host wafer, bonds a second ultra-thinned silicon layer on top, and fabricates the top transistor. While sequential processing decouples nFET and pFET thermal budgets, wafer bonding alignment precision must remain below 5nm (3-sigma) to avoid severe interconnect parasitic capacitance.

3. Thermal Dissipation in Stacked Vertical Nanostructures

A critical engineering challenge in CFET is heat extraction from the buried lower transistor. In a standard GAAFET, heat dissipates directly into the underlying bulk silicon substrate. In a monolithic CFET, the top transistor operates over an intermediate dielectric isolation layer (SiO₂/SiN), which acts as a thermal insulator (thermal conductivity ~1.4 W/m-K vs ~148 W/m-K for bulk Si).

Under high-frequency switching at 4.5 GHz, self-heating in the top nanosheet can induce thermal runaway, increasing junction temperatures by 28°C to 42°C over equivalent FinFET designs. Foundries mitigate this using ultra-thin high-thermal-conductivity AlN (aluminum nitride) middle isolation layers ($k \sim 150$ W/m-K) and routing backside power rails to act as secondary thermal sinks.

4. Middle-of-Line (MOL) Routing and Dual Backside Interconnects

Interconnecting the stacked gates and sources/drains creates extreme contact complexity. The middle-of-line (MOL) metallization must reach the bottom transistor without shorting the top gate. This is solved by combining Backside Power Delivery (BSPDN) with Frontside Signal Routing: VDD and VSS power rails are supplied from the polished wafer backside directly to the bottom nFET, while frontside BEOL metal layers route logic signals to the top pFET.

CRITICAL ENGINEERING TAKEAWAYS & DEPLOYMENT DIRECTIVES:

1. CFET achieves an immediate 50% standard cell footprint reduction by vertically stacking nFET and pFET nanosheets.
2. Monolithic CFET avoids wafer bonding alignment errors but demands extreme 100nm+ high-aspect-ratio selective etching.
3. Buried bottom transistors require high-thermal-conductivity AlN dielectric layers to prevent 35°C thermal self-heating penalties.
4. Commercial implementation at the A14/A10 nodes (2026-2028) mandates Backside Power Delivery for bottom-contact routing.